REMARKS

The present invention is a receiver and a method of data reception. In accordance with the invention, a memory 114, including an addressable storage array, stores a sequence of data samples contained in a time division multiplexed signal, as illustrated in Fig. 3. The time division multiplexed signal is from a plurality of channels in the incoming data sequence 202. Each successive data sample belongs to a channel different from a channel to which an immediately preceding data sample belongs. The memory outputs the stored data samples in a sequence of data groups equal in number to the number of channels, which in the example of Fig. 3, is five. Each data group has a plurality of samples as illustrated in Fig. 3. The contents of the memory 114, which are read in as a sequence of data samples from different channels, are read out as a sequence of data groups, as illustrated in the bottom of Fig. 3. Thereafter a decoder, as exemplified by decoder 116 in Fig. 2, which is responsive to the sequence of data groups, decodes the data samples within the sequence of data groups and outputs the decoded data samples of the plurality of data groups from the plurality of channels.

This architecture has distinct advantages over the prior art of Fig. 1. As described in Applicants' specification with reference to Fig. 1, the prior art hardware identified by reference numeral 10 requires replication for each channel.

In contrast, the present invention has an exemplary architecture illustrated in Fig. 2 which utilizes only a single memory 114 and an inner decoder 116 to achieve partial decoding of data for the R channels of Fig. 1. The present invention requires substantially less hardware requirements than the prior art. See Applicant's specification, beginning on page 17, line 9, for a discussion regarding the hardware reduction achieved by the present invention.

A preferred embodiment of the present invention includes the combination of an inner decoder 116 which receives groups of most likely bits from multiple channels in combination with an outer decoder 102 which decodes the decoded most likely bits from the inner decoder and hard decisions produced by multichannel phase tracking 112. This architecture has the aforementioned reduced hardware required for performing inner and outer decoding compared to the prior art of Fig. 1. As seen from Fig. 1, each of the R decoders and modulator 10 processes a single channel output by the mode select multiplexer 18 while the present invention substantially reduces the hardware by a factor of the overall number of Z channels.

In the Advisory Action of December 24, 2002, the Examiner takes the position that "the recitation 'receiver' has not been given patentable weight because the recitation occurs in the preamble". Independent claims 1 and 17 have been amended and newly submitted independent claims 34 and 35 have been drafted to positively recite a receiving function in the body of the claim which precludes the Examiner's interpretation of giving no patentable weight to

the Applicants' arguments regarding a receiver. Accordingly, the Applicants' arguments set forth in the December 10, 2002 Response Under 37 C.F.R. §1.116, at the top of page 4, which traversed the interpretation of Williams' coder, which is a transmitter in Fig. 10, as anticipating claims 1 and 17 are repeated. The claims, as amended, positively recite in the body in claim 1 "an input in the receiver which receives a time division multiplexed signal containing a plurality of channels which has been transmitted from a transmitter" and, in the body of claim 17, "in a receiver receiving and storing a time division multiplexed signal transmitted from a transmitter". These recitations preclude the interpretation of the claims made by the Examiner in Section 1 of the Response to Arguments in the Advisory Action.

The Examiner states in Section 2 of the Advisory Action, as follows:

> 2. As per the argument about receiver for claim 17 which also applies to claim 1, applicant's argument that figure 10 is a transmitter and not a receiver because it has a coder is incorrect. Fig. 10 may be a transmitter but it is also a receiver since it is receiving data. Just because fig. 10 is a transmitter does not preclude it from also being a receiver.

This argument is not understood by the Applicants. The Examiner cannot point to any aspect of the operation of Fig. 10 that disputes its described function as a coder. Claims 1 and 17 are limited to specific aspects of a receiver or a method in a receiver which is not met by the Examiner's assertion that Fig. 10 receives data. If the Examiner wishes to take the position that the input of data makes Fig. 10 a receiver, it is requested that he start with the input of data in Fig. 10 and read all of the elements of

claims 1 and 17 on Fig. 10. For anticipation by Williams et al the Examiner must find all of the limitations of claims 1, 13 and 17 therein.

Moreover, the Examiner's interpretation set forth in the restatement of the rejection of claims 1, 13 and 17 being anticipated by United States Patent 5,448,592 (Williams) erroneously relies upon an interpretation of a modulator as being a decoder. A person of ordinary skill in the art does not consider a modulator to be a "decoder". The Examiner has provided no basis in the record why Williams modulator could be considered a decoder. The process of decoding is not modulation and it is improper from the perspective of a person of ordinary skill in the art to interpret a modulator as a decoder. These same arguments are applicable to claims 13 and 17.

In section 3 of the Advisory Action the Examiner states as follows:

> 3. As per applicant's argument that time division multiplexing mentioned in Williams' claim 13 is not applicable to Williams's fig. 10, it is noted that Williams's claim 13 is dependent on Williams's claim 10 which is dependent on Williams's claim 1. Williams claim 1 reads on Williams's fig. 10. Therefore, Williams's claim 13 can apply to the same embodiment of Williams's fig. 10.

The disclosure of time multiplexing set forth in Williams et al is in column 15, lines 16-23, as follows:

> In the present proposal synchronizing is provided in the manner described above, and a secondary channel is provided--either using the synchronizing symbol as suggested earlier, or by multiplexing the secondary channel with the data to be transmitted. Whether block or convolutional coding is used the synchronization signals serve to permit separation of the secondary channel bits at the receiving end.

As is seen, what is discussed about multiplexing is multiplexing the secondary channel with the data to be transmitted. This description of time division multiplexing does not meet the recitation in independent claims 1 and 17 regarding multiplexing which recite "a sequence of data samples stored in the time division multiplexed signal from the plurality of channels with each successive data sample belonging to a channel different from a channel to which an immediately preceding data sample belongs". This subject matter is not met by the disclosed secondary signal described in the aforementioned portion of Williams et al upon which the multiplexing is readable of claim 13.

Moreover, claim 13 merely broadly recites "time division multiplex means" which under the sixth paragraph of 35 U.S.C. §112 must cover the corresponding structure, material or acts in the specification of Williams et al. Assuming that the aforementioned portion of column 15 discloses any structure, such structure does not correspond to the claimed time division multiplexing of claims 1, 13 and 17 which is specific to plural channels with each successive data sample belonging to a channel different from a channel to which an immediately preceding data sample belongs. The general means plus function recitation in claim 13 of time division multiplexing does not read upon or suggest the claimed subject matter of claims 1, 13, and 17 regarding multiplexing incorporated into the coder of Fig. 10.

In summary, the Examiner has the burden of demonstrating that every element of rejected claims 1, 13 and 17 are anticipated. As pointed out above, Williams et al in Fig. 10 or in claim 13, does not teach the combination of the elements recited in independent claims 1, 13 and 17, including the time division multiplexed signal as specifically recited and furthermore, a decoder which, as stated above, cannot be read upon a modulator.

Dependent claim 2 and dependent claim 18 further recite multichannel phase tracking which processes the data groups from the plurality of channels to output from each group a group of most likely bits and wherein the data samples each comprise orthogonally encoded data; and the decoder is a biorthogonal inner code soft decision data decoder which decodes the groups of the most likely bits. The Examiner's discussion in Section 9 of the Advisory Action regarding the rejection of claims 2-12, 14-16 and 18-29 alludes to orthogonally encoded data instead of convolutionally encoded data. It is requested that the Examiner state how this is relevant to the claimed inner decoder. In any event, claims 2 and 18 recite the combination of a multiphase tracking which processes the data groups from the plurality of channels to output for each data group a group of most likely bits and further, that the decoder is a biorthogonal inner code soft decision decoder which decodes the groups of most likely bits which are the output of the multiphase tracking. There is no counterpart of this combination in Williams et al.

Newly submitted claims 30 and 31 and claims 32 and 33 respectively limit claims 2 and claim 18 by reciting an outer decoder, coupled to the inner decoder, which sequentially decodes blocks of data including the most likely bits from the plurality of channels and the multiphase tracking outputs hard decisions from the multiple channels which are coupled to the outer decoder and the blocks of data include the hard decisions. This subject matter has no counterpart in Williams et al. The claimed multichannel phase tracking, inner decoding and sequential decoding of the blocks of data provides the hardware savings discussed above with regard to the improvements provided by the architecture of Fig. 2 of the present invention in comparison to the admitted prior art of Fig. 1. This architecture provides a distinct hardware savings by the claimed processing of multiple channels which has not counterpart in Williams et al.

Dependent claims 9-12 and 23-25 further limit the receiver of claim 1 and the method of claim 17 in reciting a channelizer coupled to the transmitted data and to the memory which is responsive to an input bandwidth which divides the input bandwidth into the plurality of output channels each of equal bandwidth with one of the output channels comprising the time division multiplexed signal. This architecture has the benefits of Fig. 2 as described with respect to the prior art of Fig. 1. The Examiners' reliance of the register 26 of Fig. 11 of Williams et al as a channelizer is erroneous since the function of the register 26 is to combine

smaller words of sixteen bits into a larger 32 bit word. This combining of a smaller word into a larger word is the opposite of the claimed channelizer which recites dividing the input bandwidth. Since the claimed channelizer is recited as dividing the input bandwidth into a plurality of output channels each of equal bandwidth, the "data 1" of Fig. 10 must be interpreted to be the time multiplexed signal from a channelizer in view of the independent claims requiring the time division multiplexed signal to be an input in the receiver. The register 26 of Williams et al is not associated with the input "data 1".

Newly submitted claims 34 and 35 respectively claim a satellite data reception system and a method of receiving data in a satellite which is drawn to the preferred embodiment of the present invention as described in Fig. 2. Each of claims 34 and 35 are supported by the function of the disclosed channelizer 106, multiple channel phase tracking 112, a first memory which corresponds to the memory 114, an inner decoder which corresponds to the inner coder 116, a second memory which corresponds to the block buffer RAM 130, and an outer decoder which corresponds to the outer decoder 102. Williams et al do not disclose this combination of channelizer, a multichannel phase tracking, the first and second memories and the inner and outer decoders including the recited functions.

In view of the foregoing amendments and remarks, it is submitted that the application is in condition for allowance.

To the extent necessary, Applicants petition for an extension of time under 37 C.F.R. §1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 01-2135 (199.36691X00) and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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DES:dlh

IN THE CLAIMS:

The Claim Status is as follows. Claims 1-4, 7, 9-12, 15, 17-25, and 29 are amended as follows:

1. (Currently Amended) A receiver comprising:

an input in the receiver which receives a time division multiplexed signal containing a plurality of channels which has been transmitted from a transmitter;

a memory coupled to the input, including an addressable storage array which stores a sequence of data samples contained in ~~a~~ the time division multiplexed signal from ~~a~~ the plurality of channels with each successive data sample belonging to a channel different than a channel to which an immediately preceding data sample belongs and outputs the stored data samples in a sequence of data groups equal in number to a number of the plurality of channels with each data group containing a plurality of samples from one of the plurality of channels; and

a decoder, responsive to the sequence of data groups, which decodes the data samples within the sequence of data groups and outputs decoded data samples of the plurality of data groups from the plurality of channels.

2. (Currently Amended) A receiver in accordance with claim 1 ~~wherein~~comprising:

a multichannel phase tracking which processes the data groups from the plurality of channels to output from each data group a group of most likely bits; and wherein

the data samples each comprise orthogonally encoded data; and

the decoder is a biorthogonal inner code soft decision data decoder which decodes groups of most likely bits.

3. (Currently Amended) A receiver in accordance with claim ~~2~~30 wherein:

the biorthogonal inner code soft decision data decoder is a Reed-Muller decoder.

4. (Currently Amended) A receiver in accordance with claim ~~2~~3 wherein:

the orthogonally encoded data samples are QPSK encoded.

5. (Original) A receiver in accordance with claim 1 wherein:

the receiver is contained in a satellite.

6. (Original) A receiver in accordance with claim 2 wherein:

the receiver is contained in a satellite.

7. (Currently Amended) A receiver in accordance with claim ~~3~~30 wherein:

the receiver is contained in a satellite.

8. (Original) A receiver in accordance with claim 3 wherein:

the receiver is contained in a satellite.

9. (Currently Amended) A receiver in accordance with claim 5 further comprising:

a channelizer coupled to the input and to the memory, which is responsive to an input bandwidth and which divides the input bandwidth into a plurality of output channels each of equal bandwidth, one of the output channels comprising the time division multiplexed signal.

10. (Currently Amended) A receiver in accordance with claim 6 further comprising:

a channelizer coupled to the input and to the memory, which is responsive to an input bandwidth and which divides the input bandwidth into a plurality of output channels each of equal bandwidth, one of the output channels comprising the time division multiplexed signal.

11. (Currently Amended) A receiver in accordance with claim 7 further comprising:

a channelizer coupled to the input and to the memory, which is responsive to an input bandwidth and which divides the input bandwidth into a plurality of output channels each of equal bandwidth, one of the output channels comprising the time division multiplexed signal.

12. (Currently Amended) A receiver in accordance with claim 8 further comprising:

a channelizer coupled to the input and the memory, which is responsive to an input bandwidth and which divides the input bandwidth into a plurality of output channels each of equal bandwidth, one of the output channels comprising the time division multiplexed signal.

13. (Original) A receiver in accordance with claim 1 wherein:

the memory comprises a write address generator and a read address generator and the addressable storage array contains memory cells which are addressed by addresses generated by the write address generator and the read address generator, the sequence of data samples being written in a group of memory cells with addresses generated by the write address generator, and the sequence of data groups being read out with addresses generated by the read address generator.

14. (Original) A receiver in accordance with claim 2 wherein:

the memory comprises a write address generator and a read address generator and the addressable storage array contains memory cells which are addressed by addresses generated by the write address generator and the read address generator, the sequence of data samples being written in a group of memory cells with addresses generated by the write address generator, and the sequence of data groups being read out with addresses generated by the read address generator.

15. (Currently Amended) A receiver in accordance with claim ~~5~~30 wherein:

the memory comprises a write address generator and a read address generator and the addressable storage array contains memory cells which are addressed by addresses generated by the write address generator and the read address generator, the sequence of data samples being written in a group of memory cells with addresses generated by the write address generator, and the sequence of data groups being read out with addresses generated by the read address generator.

16. (Original) A receiver in accordance with claim 5 wherein:

each of the at least one memory further comprises a write address generator and a read address generator and the addressable storage array

contains memory cells which are addressed by addresses generated by the write address generator and the read address generator, the sequence of data samples being written in a group of the memory cells with addresses generated by the write address generator and the sequence of data groups being read out with addresses generated by the read address generator;

the another memory further comprises a write address generator and a read address generator and the addressable storage array contains memory cells which are addressed by addresses generated by the write address generator and the read address generator, the sequence of data samples being written in a group of the memory cells of the another memory with addresses generated by the write address generator and the sequence of data groups being read out from a group of memory cells of the another memory with addresses generated by the read address generator.

17. (Currently Amended) A method of data reception comprising:

in a receiver receiving and storing a time division multiplexed signal transmitted from a transmitter containing a sequence of data samples from a plurality of channels with each successive data sample belonging to a channel different than a channel to which an immediately preceding data sample belongs;

outputting the stored data samples in a sequence of data groups equal in number to a number of the plurality of channels, each data group containing a plurality of samples from one of the plurality of channels;

decoding the data samples within the sequence of data groups; and

outputting the decoded data samples of the plurality of data groups from the plurality of channels .

18. (Currently Amended) A method in accordance with claim ~~18~~17 wherein:

performing multiphase tracking of the data groups from the plurality of channels to output from each group a group of most likely bits; and wherein

the data samples each comprise orthogonally encoded data; and

the decoder is an inner code soft decision biorthogonal decoder which decodes groups of most likely bits.

19. (Currently Amended) A method in accordance with claim ~~18~~32 wherein:

the orthogonally encoded data samples are QPSK encoded.

20. (Currently Amended) A method in accordance with claim 17 wherein:

the ~~data is received by~~ receiver is contained in a satellite.

21. (Currently Amended) A method in accordance with claim 18 wherein:

the ~~data is received by~~ receiver is contained in a satellite.

22. (Currently Amended) A method in accordance with claim ~~19~~32 wherein:

the ~~data is received by~~ receiver is contained in a satellite.

23. (Currently Amended) A method in accordance with claim 20 wherein:

an input bandwidth from the transmitter is received by the receiver and is divided by the receiver with a channelizer into a plurality of output channels each of equal bandwidth, one of the output channels comprising the time division multiplexed signal.

24. (Currently Amended) A method in accordance with claim 21 wherein:

an input bandwidth from the transmitter is received by the receiver and is divided by the receiver with a channelizer into a plurality of output channels each of equal bandwidth, one of the output channels comprising the time division multiplexed signal.

25. (Currently Amended) A method in accordance with claim 22 wherein:

an input bandwidth from the transmitter is received by the receiver and is divided by the receiver with a channelizer into a plurality of output channels each of equal bandwidth, one of the output channels comprising the time division multiplexed signal.

26. (Original) A method in accordance with claim 20 further comprising:

addressing memory cells of each of the at least one memory by addresses generated by a read address generator and a write address generator, the sequence of data samples being written in a data group of memory cells by addresses generated by the write address generator and the sequence of data groups individually outputted from a group of memory cells being generated by addresses generated by the read address generator.

27. (Original) A method in accordance with claim 21 further comprising:

addressing memory cells of each of the memories and the another memory by addresses generated by write address generators and read address generators, the sequence of data samples being written in a group of memory cells by addresses generated by the write address generators and the sequence of data groups outputted from the memories and the another memory being generated by addresses generated by the read address generators.

28. (Original) A method in accordance with claim 22 further comprising:

addressing memory cells of each of the at least one memory by addresses generated by a read address generator and a write address generator, the sequence of data samples being written in a data group of memory cells by addresses generated by the write address generator and the sequence of data groups individually outputted from a group of memory cells being generated by addresses generated by the read address generator.

29. (Currently Amended) A method in accordance with claim ~~23~~32 wherein:

the data samples are stored in an addressable storage array containing memory cells which are addressed by a pair of addresses, the sequence of data samples being written in a group of memory cells each containing one common address of the pair of addresses and the sequence of data groups are each individually outputted from a group of memory cells containing one common address which is another of the pair of addresses.

Please insert new claims 30-35 as follows:

30. (New) A receiver in accordance with claim 2 comprising:

an outer decoder, coupled to the inner decoder, which sequentially decodes blocks of data including the most likely bits from the plurality of channels.

31. (New) A receiver in accordance with claim 30 wherein:

the multichannel phase tracking outputs hard decisions from the multiple channels which are coupled to the outer decoder and the blocks of data include the hard decisions which are also decoded by the outer decoder.

32. (New) A method in accordance with claim 18 comprising:

sequentially decoding blocks of data including the most likely bits from the plurality of channels.

33. (New) A method in accordance with claim 32 wherein:

the multichannel phase tracking outputs hard decisions from multiple channels which are coupled to the outer decoder and the blocks of data include the hard decisions which are also decoded by the outer decoder.

34. (New) A satellite data reception system comprising:

a channelizer which receives a frequency spectrum containing samples of a band transmitted from a transmitter over a wireless link and divides the frequency spectrum into subbands including a sequence of the data samples comprising a time division multiplexed signal from multiple channels output by the channelizer with each successive data sample belonging to a channel different from a channel to which an immediately preceding data sample belongs;

a multiple channel phase tracking coupled to the time division multiplexed signal from the multiple channels which outputs sequentially groups of most likely bits and from hard decisions from multiple channels;

a first memory, coupled to groups of most likely bits, which stores the groups of most likely bits from the multiple channels and outputs a sequence of data groups equal to a number of the multiple channels with each data group containing a plurality of samples from one of the multiple channels;

an inner decoder, responsive to the sequence of data groups from the first memory, which outputs decoded data groups from the multiple channels;

a second memory, coupled to the decoded data groups from the multiple channels and to the hard decisions from multiple channels, which stores the decoded data groups and the hard decisions into data blocks which are sequentially output by the second memory; and

an outer decoder which decodes the sequentially output data blocks from the second memory.

35. (New) A method of receiving data in a satellite which is transmitted from a transmitter over a wireless link that is received with a data receiving system including a channelizer, a multiple channel phase tracker, a first memory, an inner decoder, a second memory and an outer decoder comprising:

receiving with the channelizer a frequency spectrum containing data samples transmitted from the transmitter and dividing the frequency spectrum into subbands, including a sequence of data samples comprising a time division multiplexed signal output from multiple channels with each successive data sample belonging to a channel different from a channel to which an immediate preceding data sample belongs;

the multiple channel phase tracking in response to the time division multiplexed signal from the multiple channels sequentially outputs groups of most likely bits and hard decisions from the multiple channels;

storing with the first memory groups of most likely bits from the multiple channels and outputting a sequence of data groups equal to a number of

the multiple channels with each data group containing a plurality of samples from one of the multiple channels;

the inner decoder, in response to the output of data groups from the first memory, outputs decoded data groups from the multiple channels;

the second memory in response to the decoded data groups and to the hard decisions, stores and sequentially outputs the decoded data groups and the hard decisions into data blocks; and

the outer decoder, in response to the sequential output of the stored data blocks from the second memory, sequentially decodes the data blocks.